The EXA-DUNE project
Dune vs. 1 000 000 000 000 000 000 000

Christian Engwer
joint work with P. Bastian, O. Ippisch, J. Fahlke, D. Göddeke, S. Müthing, D. Ribbrock, S. Turek

2.04.2016, OPM Meeting
2006 Discussion in the German Research Foundation (DFG) on the necessity of a funding initiative for HPC software.

2010 Discussion with DFG’s Executive Committee. Suggestion of a flexible, strategically initiated SPP. Initiative out of Germany HPC community, referring to increasing activities on HPC software elsewhere (USA: NSF, DOE; Japan; China; G8)

2011 Submission of the proposal, international reviewing, and formal acceptance.

2012 13 full proposals accepted for funding SPPEXA 1. Review of project sketches and full proposals.

2013 Official start of SPPEXA 1.

2014 Call for proposals SPPEXA 2, incl. international partners (France, Japan)

2015 16 full proposals accepted for funding SPPEXA 2 (7 collaborations with Japan / 3 collaborations with France).

2016 Official start of SPPEXA 2.

2020 Expected arrival of EXA-scale machines ;–)
2006 Discussion in the German Research Foundation (DFG) on the necessity of a funding initiative for HPC software.

2010 Discussion with DFG’s Executive Committee. Suggestion of a flexible, strategically initiated SPP. Initiative out of Germany HPC community, referring to increasing activities on HPC software elsewhere (USA: NSF, DOE; Japan; China; G8).

2011 Submission of the proposal, international reviewing, and formal acceptance.

2012 13 full proposals accepted for funding SPPEXA 1. Review of project sketches and full proposals.

2013 Official start of SPPEXA 1.

2014 Call for proposals SPPEXA 2, incl. international partners (France, Japan).

2015 16 full proposals accepted for funding SPPEXA 2 (7 collaborations with Japan / 3 collaborations with France).

2016 Official start of SPPEXA 2.

2020 Expected arrival of EXA-scale machines ;()

6 years HPC related project funding
EXA-DUNE

DUNE’s Framework approach to software development

- Integrated toolbox of simulation components
- Existing body of complex applications
- Good performance + scalability for traditional MPI model
Challenges:

▶ Standard low order algorithms do not scale any more
▶ Incorporate new algorithms, hardware paradigms
▶ Integrate changes across simulation stages (Ahmdahl’s Law)
▶ Provide “reasonable” upgrade path for existing applications
DUNE + FEAST = Flexibility + Performance

- General Software Frameworks
  - co-designed to specific hardware platforms is not sufficient

- Hardware-Oriented Numerics
  - design/choose algorithms with hardware in mind
Hardware Challenges

- Multiple Levels of concurrency
- MPI-parallel, Multi-core, SIMD
- Memory-wall
Hardware Challenges

- Multiple Levels of concurrency
- MPI-parallel, Multi-core, SIMD
- Memory-wall

Example Intel Xeon E5-2698v3 (Haswell)
- Advertised peak performance: 486.4 GFlop/s
Hardware Challenges

- Multiple Levels of concurrency
- MPI-parallel, Multi-core, SIMD
- Memory-wall

**Example** Intel Xeon E5-2698v3 (Haswell)

- Advertised peak performance: 486.4 GFlop/s
- 16 cores → single Core: 30.4 GFlop/s
Hardware Challenges

- Multiple Levels of concurrency
- MPI-parallel, Multi-core, SIMD
- Memory-wall

Example Intel Xeon E5-2698v3 (Haswell)
- Advertised peak performance: 486.4 GFlop/s
- 16 cores → single Core: 30.4 GFlop/s
- AVX2+FMA → without FMA: 15.2 GFlop/s
Hardware Challenges

- Multiple Levels of concurrency
- MPI-parallel, Multi-core, SIMD
- Memory-wall

Example Intel Xeon E5-2698v3 (Haswell)

- Advertised peak performance: 486.4 GFlop/s
- 16 cores → single Core: 30.4 GFlop/s
- AVX2+FMA → without FMA: 15.2 GFlop/s
- 4× SIMD → without AVX: 3.8 GFlop/s

→ classic, non-parallel code bound by 3.8 GFlop/s
→ you loose 99% Performance
Outline

1. Introduction
2. EXA-DUNE Overview
3. EXA-DUNE Selected Features
   - Linear Algebra
   - Assembly
   - High-level SIMD techniques
   - Multiple RHS
4. Outlook
Hybrid Parallelism

- Coarse-grained: MPI between heterogeneous nodes
- Medium-grained: multicore-CPU, GPUs, MICs, APUs, ...
- Fine-grained: vectorization, GPU ‘threads’, ...
Hybrid Parallelism

- **Coarse-grained**: MPI between heterogeneous nodes
- **Medium-grained**: multicore-CPU, GPUs, MICs, APUs, … TBB
- **Fine-grained**: vectorization, GPU ‘threads’, …???
Algorithm Design
Hardware-Oriented Numerics

Challenge: Combine flexibility and hardware efficiency
- Existing codes no longer run faster automatically
- Standard low order algorithms do not scale any more
- *Much more than a pure implementational issue*
Algorithm Design
Hardware-Oriented Numerics

**Challenge**: Combine flexibility and hardware efficiency

**Solution**: Locally structured, globally unstructured data
→ *increased algorithmic intensity* and *vectorization*

**Concepts:**
- **higher order**: Discontinuous Galerkin, Reduced Basis
- **virtual local refinement**: global unstructured mesh, local tensor-product mesh
- **multiple right-hand-sides**: horizontal SIMD-vectorization
Algorithm Design
Hardware-Oriented Numerics

Challenge: Combine flexibility and hardware efficiency

Solution: Locally structured, globally unstructured data
→ *increased algorithmic intensity and vectorization*

Concepts:

- higher order:
  Discontinuous Galerkin, Reduced Basis
- virtual local refinement:
  global unstructured mesh, local tensor-product mesh
- multiple right-hand-sides:
  horizontal SIMD-vectorization
Algorithm Design
Hardware-Oriented Numerics

Challenge: Combine flexibility and hardware efficiency

Solution: Locally structured, globally unstructured data → *increased algorithmic intensity and vectorization*

Concepts:

▶ higher order: Discontinuous Galerkin, Reduced Basis

▶ virtual local refinement: global unstructured mesh, local tensor-product mesh

▶ multiple right-hand-sides: horizontal SIMD-vectorization

\[
\begin{pmatrix}
  x_{0,0} & x_{1,0} & \ldots & x_{N,0} \\
  x_{0,1} & x_{1,1} & \ldots & x_{N,1} \\
  x_{0,2} & x_{1,2} & \ldots & x_{N,2} \\
  \vdots & \vdots & \ddots & \vdots \\
  x_{0,M} & x_{1,M} & \ldots & x_{N,M}
\end{pmatrix}
\cdot
\begin{pmatrix}
  b_{0,0} & b_{1,0} & \ldots & b_{N,0} \\
  b_{0,1} & b_{1,1} & \ldots & b_{N,1} \\
  b_{0,2} & b_{1,2} & \ldots & b_{N,2} \\
  \vdots & \vdots & \ddots & \vdots \\
  b_{0,M} & b_{1,M} & \ldots & b_{N,M}
\end{pmatrix}
\]
Features in EXA-DUNE

dune-common
▶ Multi-Threading support in DUNE (via TBB)

dune-grid
▶ Hybrid parallelization of DUNE grids (on-top of the grid interface)
▶ Virtual-refinement of unstructured DUNE grids

dune-istl
▶ Hybrid parallelization
▶ Performance portable Matrix format
▶ (vertically) vectorized preconditioners (incl. CUDA versions)
▶ (horizontally) vectorized solvers (multiple RHS)

dune-pdelab
▶ Sum-Factorization DG
▶ Special-purpose high-performance assemblers
Features in EXA-DUNE

dune-common
  ▶ Multi-Threading support in DUNE (via TBB)
dune-grid
  ▶ Hybrid parallelization of DUNE grids (on-top of the grid interface)
  ▶ Virtual-refinement of unstructured DUNE grids
dune-istl
  ▶ Hybrid parallelization
  ▶ Performance portable Matrix format
  ▶ (vertically) vectorized preconditioners (incl. CUDA versions)
  ▶ (horizontally) vectorized solvers (multiple RHS)
dune-pdelab
  ▶ Sum-Factorization DG
  ▶ Special-purpose high-performance assemblers
SELL-C-\(\sigma\) as Cross-Platform Matrix Format

Kreutzer, Hager, Wellein, Fehske, Bishop ’13

Block-sorted and chunked ELL (SELL-C-\(\sigma\)) with suitable tuning offers competitive performance across modern architectures (CPU, GPGPU, Xeon Phi)

- Adopt SELL-C-\(\sigma\) as unified matrix format in DUNE (including assembly phase → dune-pdelab)
- Differentiate by memory domain (host, Xeon Phi, GPU)
- Memory domain and C via extended C++ allocator interface
Blocked SELL Format for DG discretizations

Choi, Singh, Vuduc ’10

Interleaved storage of blocks from $C$ block rows

- Move SIMD from scalar level to block level
- Vectorize algorithms by operating on *multiple independent blocks* simultaneously
- Tradeoff between vectorization and cache usage at larger block sizes

[Muething et.al. 2013]
Hybrid-parallel DUNE Grid

Strategies for multi-threaded assembly of matrices and vectors

- Thread parallelization on-top of the DUNE grid interface

- Evaluation of partitioning strategies:
  - strided
  - ranged
  - sliced
  - tensor

- ... and data access strategies:
  - batched: Batched writeback with global lock.
  - elock: One lock per mesh entity
  - coloring: partitions of the same color do not “touch”.

Other strategies not considered here:
- global locking → as bad as expected.
- race-free schemes → in general not possible not possible.
Evaluation

Evaluation of partitioning strategies

» Best partitioning strategy: ranges of cells
  → memory efficient and fast

... and data access strategies

» Best strategy: entity-wise locking
  (no benefit from coloring)

<table>
<thead>
<tr>
<th>$k$</th>
<th>$E_{CPU}^{10}$</th>
<th>$E_{CPU}^{20}$</th>
<th>$E_{PHI}^{60}$</th>
<th>$E_{PHI}^{120}$</th>
<th>$E_{PHI}^{240}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>62%</td>
<td>42%</td>
<td>75%</td>
<td>43%</td>
<td>21%</td>
</tr>
<tr>
<td>1</td>
<td>62%</td>
<td>42%</td>
<td>84%</td>
<td>57%</td>
<td>30%</td>
</tr>
<tr>
<td>2</td>
<td>72%</td>
<td>46%</td>
<td>90%</td>
<td>69%</td>
<td>38%</td>
</tr>
<tr>
<td>3</td>
<td>79%</td>
<td>50%</td>
<td>92%</td>
<td>72%</td>
<td>41%</td>
</tr>
<tr>
<td>4</td>
<td>87%</td>
<td>49%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>88%</td>
<td>51%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Runtimes per dof, degree $k$, jacobian, sliced partitioning, entity-wise locking

Evaluation: 60-core Xeon PHIs and 10-core CPU’s

» Full benefit of Xeon PHI will require vectorization of user code
  → vectorization: non-trivial, work in progress
Evaluation of partitioning strategies

- Best partitioning strategy: ranges of cells
  → memory efficient and fast

... and data access strategies

- Best strategy: entity-wise locking
  (no benefit from coloring)

<table>
<thead>
<tr>
<th>$k$</th>
<th>$E_{10}^{\text{CPU}}$</th>
<th>$E_{20}^{\text{CPU}}$</th>
<th>$E_{60}^{\text{PHI}}$</th>
<th>$E_{120}^{\text{PHI}}$</th>
<th>$E_{240}^{\text{PHI}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>62%</td>
<td>42%</td>
<td>75%</td>
<td>43%</td>
<td>21%</td>
</tr>
<tr>
<td>1</td>
<td>62%</td>
<td>42%</td>
<td>84%</td>
<td>57%</td>
<td>30%</td>
</tr>
<tr>
<td>2</td>
<td>72%</td>
<td>46%</td>
<td>90%</td>
<td>69%</td>
<td>38%</td>
</tr>
<tr>
<td>3</td>
<td>79%</td>
<td>50%</td>
<td>92%</td>
<td>72%</td>
<td>41%</td>
</tr>
<tr>
<td>4</td>
<td>87%</td>
<td>49%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>88%</td>
<td>51%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Runtimes per dof, degree $k$, jacobian, sliced partitioning, entity-wise locking

Evaluation: 60-core Xeon PHIs and 10-core CPU’s

- Full benefit of Xeon PHI will require vectorization of user code
  → vectorization: non-trivial, work in progress
Vectorizing over Elements

*User provides local Operator to compute local Stiffness matrix*

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality
Vectorizing over Elements

_user provides local Operator to compute local Stiffness matrix_

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality

Local coefficients vector:
- $v_0$, $v_1$, $v_2$, $v_3$

Patch coefficients vector:
- $0.0$, $1.0$, $2.0$, $3.0$, $0.1$, $1.1$, $2.1$, $3.1$, $0.2$, $1.2$, $2.2$, $3.2$, $0.3$, $1.3$, $2.3$, $3.3$, $0.4$, $1.4$, $2.4$, $3.4$
Vectorizing over Elements

User provides local Operator to compute local Stiffness matrix

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality

(1)
Vectorizing over Elements

*User provides local Operator to compute local Stiffness matrix*

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality
Vectorizing over Elements

User provides local Operator to compute local Stiffness matrix

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality
Vectorizing over Elements

*User provides local Operator to compute local Stiffness matrix*

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality

![Diagram showing patch coefficients vector and local coefficients vector]
Vectorizing over Elements

User provides local Operator to compute local Stiffness matrix

- Patch Grid
- reduce costs of unstructured meshes
  - extract subset of mesh
  - store as flat grid
  - store in consecutive arrays, without pointers
- add structured refinement
  - exploit local structure
  - improve data locality
Vectorizing over Elements (2)

\[- \Delta u = 0 \quad \text{on } \Omega + BC\]

- Conforming FEM, Lagrange, \( Q_1 \), three level virtual refinement
- 16-Core Intel Haswell E5-2698v3
  - Advertised 486.4 GFlop/s,
  - Peak w.o. FMA: 243.2 GFlop/s (\( \rightarrow \) %avail)
  - Bandwidth: STREAM \( 2 \times 40 \) GByte/s

<table>
<thead>
<tr>
<th>SIMD</th>
<th>lanes</th>
<th>threads</th>
<th>GByte/s</th>
<th>%effBW</th>
<th>GFlop/s</th>
<th>%avail</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>1</td>
<td>16</td>
<td>26.73</td>
<td>33.4</td>
<td>9.758</td>
<td>4.0</td>
</tr>
<tr>
<td>-</td>
<td>1</td>
<td>32</td>
<td>34.32</td>
<td>42.9</td>
<td>12.53</td>
<td>5.2</td>
</tr>
<tr>
<td>AVX</td>
<td>4</td>
<td>16</td>
<td>62.89</td>
<td>78.8</td>
<td>22.96</td>
<td>9.4</td>
</tr>
<tr>
<td>AVX</td>
<td>4</td>
<td>32</td>
<td>73.01</td>
<td>91.3</td>
<td>26.65</td>
<td>11.0</td>
</tr>
</tbody>
</table>
Interface Challenges

Vectorization of local operator (user code)
Interface Challenges

Vectorization of local operator (user code)

- Intrinsic (non-portable)
- Special language (needs special compiler)
- Autovectorizer (difficult to drive portably)
Interface Challenges

Vectorization of local operator (user code)

- Intrinsic (non-portable)
- Special language (needs special compiler)
- Autovectorizer (difficult to drive portably)
- Vectorization library (e.g. Vc, Boost.SIMD, NGSolve)
Programming Approaches

- Intrinsics (non-portable)
- Special language (needs special compiler)
- Autovectorize (difficult to drive portably)
Programming Approaches

- Intrinsic (non-portable)
- Special language (needs special compiler)
- Autovectorize (difficult to drive portably)

WWU Münster Christian Engwer 02.06.2016
Programming Approaches

- Intrinsic (non-portable)
- Special language (needs special compiler)
- Autovectorize (difficult to drive portably)
- Vectorization library
  - Hide intrinsics beneath a portable interface
  - Implementations: e.g. Vc, Boost.SIMD, NGSolve
Features of Vc

**Storage:** Vc::SimdArray<T,N>  
Abstracts a vector of type T with size N

**SIMD Operator overloads:** +, −, ·, /, etc.

```cpp
template <typename T>
SimdArray<T,N> operator *(SimdArray<T,N> a, SimdArray<T,N> b) {
    for (std::size_t i = 0; i < N; i++) a[i] *= b[i];
    return a;
}
```

Limitations:

- Not all operations are supported on SIMD data types
- In particular
  - No implicit cast from float → double
  - No branching, e.g. if(c) x=a else x=b
  - Alternative: `x = c?a:b;` → `x = cond(c, a, b);`
Features of Vc

Storage: Vc::SimdArray<T,N>
Abstracts a vector of type T with size N

SIMD Operator overloads: +, −, ·, /, etc.

```cpp
template <typename T>
SimdArray<T,N> operator *(SimdArray<T,N> a, SimdArray<T,N> b) {
    for (std::size_t i = 0; i < N; i++) a[i] *= b[i];
    return a;
}
```

Limitations:
Not all operations are supported on SIMD data types
In particular
- No implicit cast from float → double
- No branching, e.g. if(c) x=a else x=b
  Alternative: x = c?a:b; → x = cond(c,a,b);
Horizontal Vectorization for multiple RHS

- Many applications require solves for many right-hand-sides
  - Multi-Scale FEM
  - Inverse problems
  - ...
Horizontal Vectorization for multiple RHS

- Many applications require solves for many right-hand-sides
  - Multi-Scale FEM
  - Inverse problems
  - ...
- This corresponds to

  \[
  \text{foreach } i \in [0, N] : \text{solve } A x_i = b_i \rightarrow \text{solve } A X = B
  \]

  with \( X = (x_0, \ldots x_N) \), \( B = (b_0, \ldots b_N) \)
Horizontal Vectorization for multiple RHS

- Many applications require solves for many right-hand-sides
  - Multi-Scale FEM
  - Inverse problems
  - ...
- This corresponds to

\[
\text{foreach } i \in [0, N] : \text{solve } Ax_i = b_i \quad \rightarrow \quad \text{solve } AX = B
\]

with \( X = (x_0, \ldots x_N) \), \( B = (b_0, \ldots b_N) \)

- Templated FEM-code allows to implement vectorized assembly and solvers, e.g.

  ```cpp
  template<typename T> Dune::BlockVector
  template<class X> class BiCGSTABSolver : public InverseOperator<X,X>
  template<class M, class X, class Y> class AssembledLinearOperator
  ```
Modifications to the linear Algebra code

\[ \text{Dune::BlockVector< double >} \quad \rightarrow \quad \text{Dune::BlockVector<Vc::SimdArray<double,N>>>} \]

\[
X = \begin{pmatrix}
  x_{0,0} & x_{1,0} & x_{2,0} & \cdots & x_{N,0} \\
  x_{0,1} & x_{1,1} & x_{2,1} & \cdots & x_{N,1} \\
  x_{0,2} & x_{1,2} & x_{2,2} & \cdots & x_{N,2} \\
  \vdots & \vdots & \vdots & \ddots & \vdots \\
  x_{0,M} & x_{1,M} & x_{2,M} & \cdots & x_{N,M}
\end{pmatrix}
\]

Memory layout: Corresponds to \( M \times N \) dense-matrix with row-major storage.
Modifications to the linear Algebra code

\[
\begin{pmatrix}
  x_{0,0} & x_{1,0} & x_{2,0} & \cdots & x_{N,0} \\
  x_{0,1} & x_{1,1} & x_{2,1} & \cdots & x_{N,1} \\
  x_{0,2} & x_{1,2} & x_{2,2} & \cdots & x_{N,2} \\
  \vdots & \vdots & \vdots & \ddots & \vdots \\
  x_{0,M} & x_{1,M} & x_{2,M} & \cdots & x_{N,M}
\end{pmatrix}
\]

Memory layout: Corresponds to \( M \times N \) dense-matrix with row-major storage.

And smaller SIMD-aware modifications to the Solvers
Application: EEG Source Reconstruction

Cooperation UKM (Münster), BESA GmbH (München)

- EEG measurements
- > 200 electrodes
- measure surface potential
- governing equation

$$-\nabla \cdot K \nabla u = f \quad \text{on } \Omega$$
$$\nabla u \cdot n = 0 \quad \text{on } \partial \Omega$$

Goal: reconstruct brain activity

- Inverse modelling approach
- $L_2$ regularizer
- Fidelity term on potential at electrodes

Application: EEG Source Reconstruction

Cooperation UKM (Münster), BESA GmbH (München)

- EEG measurements
- > 200 electrodes
- measure surface potential
- governing equation

\[-\nabla \cdot K \nabla u = 0 \quad \text{on } \Omega\]
\[\nabla u \cdot n = j \quad \text{on } \partial \Omega\]

Goal: reconstruct brain activity
- Inverse modelling approach
- $L_2$ regularization
- Fidelity term on potential at electrodes
Performance Measurements

- SIMD-vectorized AMG-CG solver
- Solve for 256 RHS, 300K Cells, 60K Vertices
- Timing for Haswell-EP (E5-2698v3, 16 cores, AVX2, 4 lanes)
  - 1-16 cores
  - no SIMD, AVX (4 lanes), AVX (4 × 4 lanes)
  - speedup 50 (max theoretical speedup 64)
Outlook
Transition from EXA-DUNE to mainline?!

dune-common

▶ Multi-Threading support in DUNE (via TBB)

dune-grid

▶ Hybrid parallelization of DUNE grids (on-top of the grid interface)
▶ Virtual-refinement of unstructured DUNE grids

dune-istl

▶ Hybrid parallelization
▶ Performance portable Matrix format
▶ (vertically) vectorized preconditioners (incl. CUDA versions)
▶ (horizontally) vectorized solvers (multiple RHS)

dune-pdelab

▶ Sum-Factorization DG
▶ Special-purpose high-performance assemblers
Outlook
Transition from EXA-DUNE to mainline?!

- **dune-common**
  - Multi-Threading support in DUNE (via TBB)

- **dune-grid**
  - Hybrid parallelization of DUNE grids (on-top of the grid interface)
  - Virtual-refinement of unstructured DUNE grids

- **dune-istl**
  - Hybrid parallelization
  - Performance portable Matrix format
  - (vertically) vectorized preconditioners (incl. CUDA versions)
  - (horizontally) vectorized solvers (multiple RHS)

- **dune-pdelab**
  - Sum-Factorization DG
  - Special-purpose high-performance assemblers
Outlook II
second phase

▶ Push features upstream
▶ Task-parallel scheduling
▶ Asynchronicity → latency hiding, communication hiding, …
▶ Resilience
▶ …
Outlook II
second phase

▶ Push features upstream
▶ Task-parallel scheduling
▶ Asynchronicity → latency hiding, communication hiding, …
▶ Resilience
▶ …

Questions?!